

**Faculty of Engineering and Technology**

**Electrical and Computer Engineering Department**

**DIGITAL SYSTEMS – ENCS2340**

**Verilog HDL Project**

**BCD adder–subtractor circuit**

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**Section:** 3

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# **Abstract**

**The aim of this project:**

To implement a BCD adder—subtractor circuit by building the system components separately using Verilog HDL. Then, integrating all components to build the whole system.

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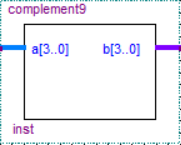
# **Procedure and Discussion**

### **Components:**

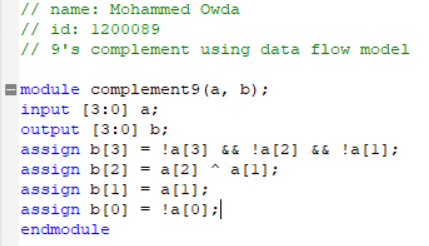
In this project, I used three main components to build an BCD adder–subtractor circuit. First, 9’s Complementer which it takes the 9’s complement of BCD number. Then, I used quadruple 2X1 multiplexer which it chooses between two 4bit numbers. Finally, I used BCD adder to find the sum of two BCD numbers.

#### 1) 9’s Complementer

9’s Complementer has four input a [3:0] that takes BCD number of 4bit and find the 9’s Complement of that number as four output b [3:0]

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##### **Code:**



##### **Simulation:**

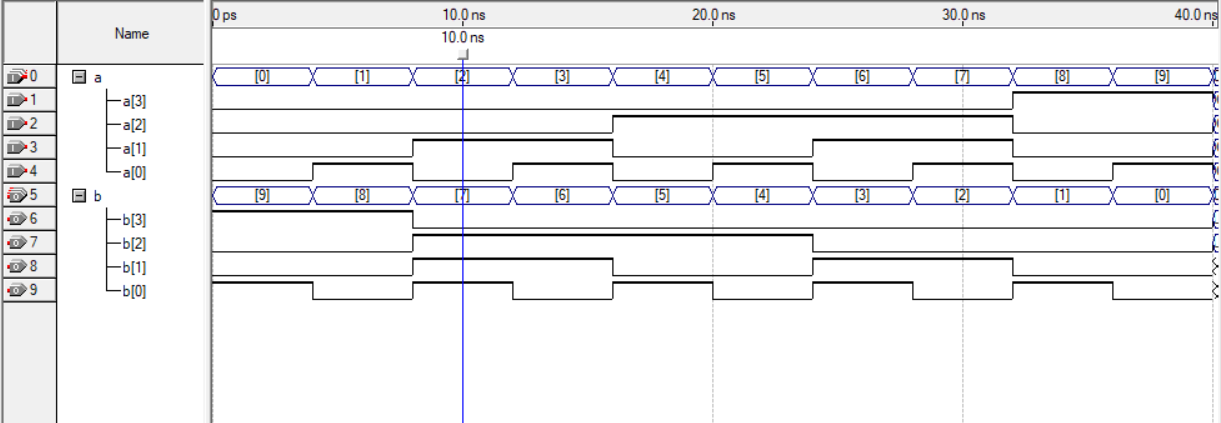
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Figure : 9’s Complementer Waves

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| A0 | A1 | A2 | A3 | B0 | B1 | B2 | B3 |
| 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| X | X | X | X  .  .  . | X | X | X | X |
| X | X | X | X | X | X | X | X |

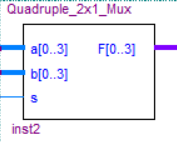
To sure that the coed is work perfectly, we check the waves. For example, if we took the inputs when it 0001 (1 in BCD) we get 1000 (8 in BCD) in the output. And if we take 0111 (7 in BCD) we get 0010 (2 in BCD), and so on.

After check all inputs we made sure that the values match with the truth table.

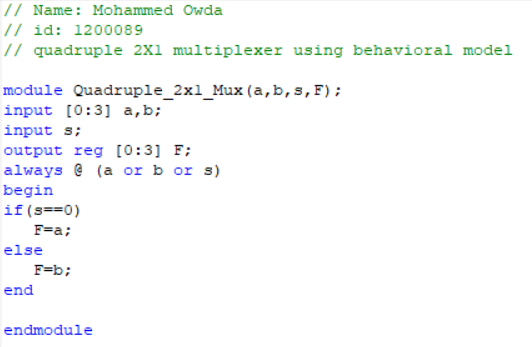
Figure : 9's Complementer truth table

#### 2) quadruple 2X1 multiplexer

This component takes eight inputs as two 4bit numbers, and it choose a number between the two numbers according to the selection input (s). And the output is just a one number of 4bit.

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##### **Code:**



##### **Simulation:**

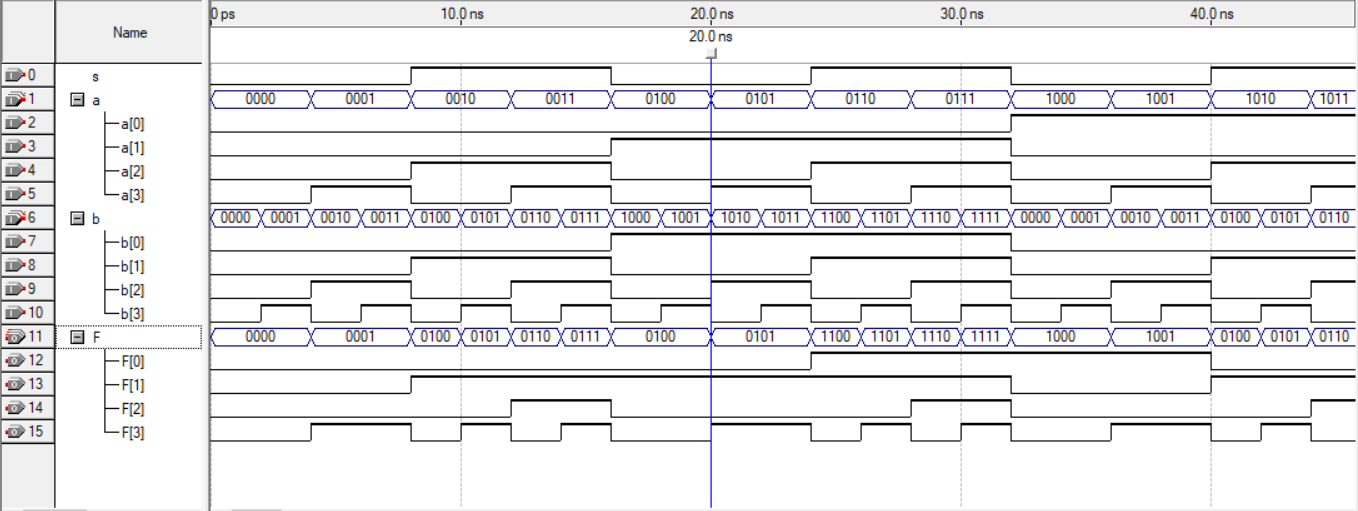


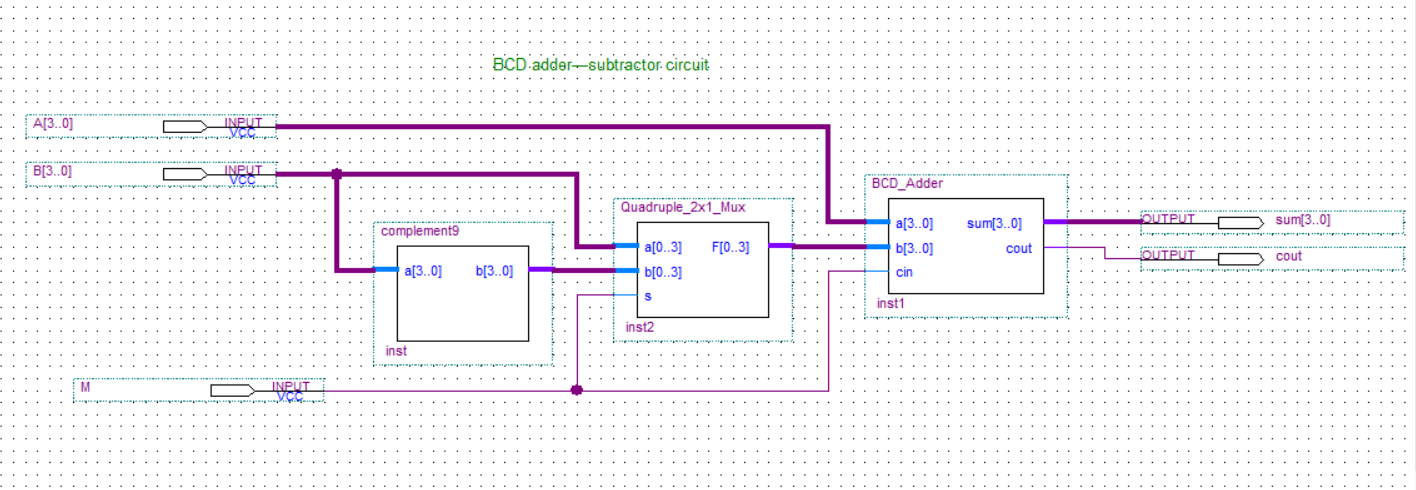
Figure : Quadruple 2x1 multiplexer Waves

To sure That the quadruple 2X1 multiplexer works perfectly, we must check if the selection equals to 0 then, we will get A, and if the selection equal to 1 we will get B in the output.

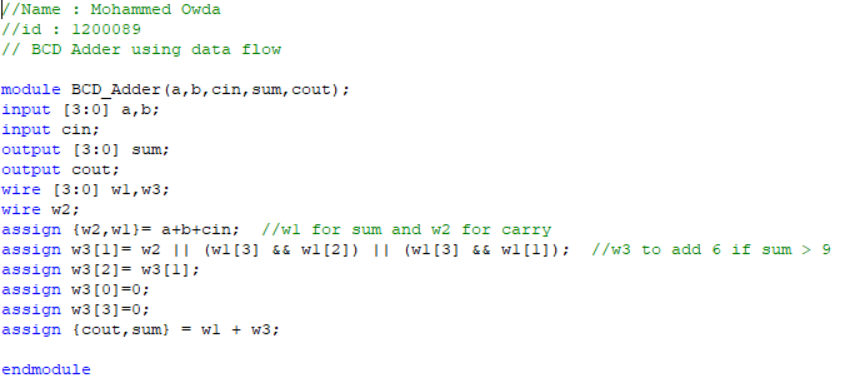
From Figure 3, when the selection s is 0, a is 0001 and b is 0010 the output 0001 which is a. And when the selection s is 1, a is 0110 and b is 1100 we get 1100 which is b. So the code works perfectly.

#### 3) BCD Adder:

BCD adder takes two BCD numbers of 4bits in addition to cin. This component finds the sum of the two BCD numbers. And it has sum and carry out as an outputs.



###### **Code:**



###### **Simulation:**

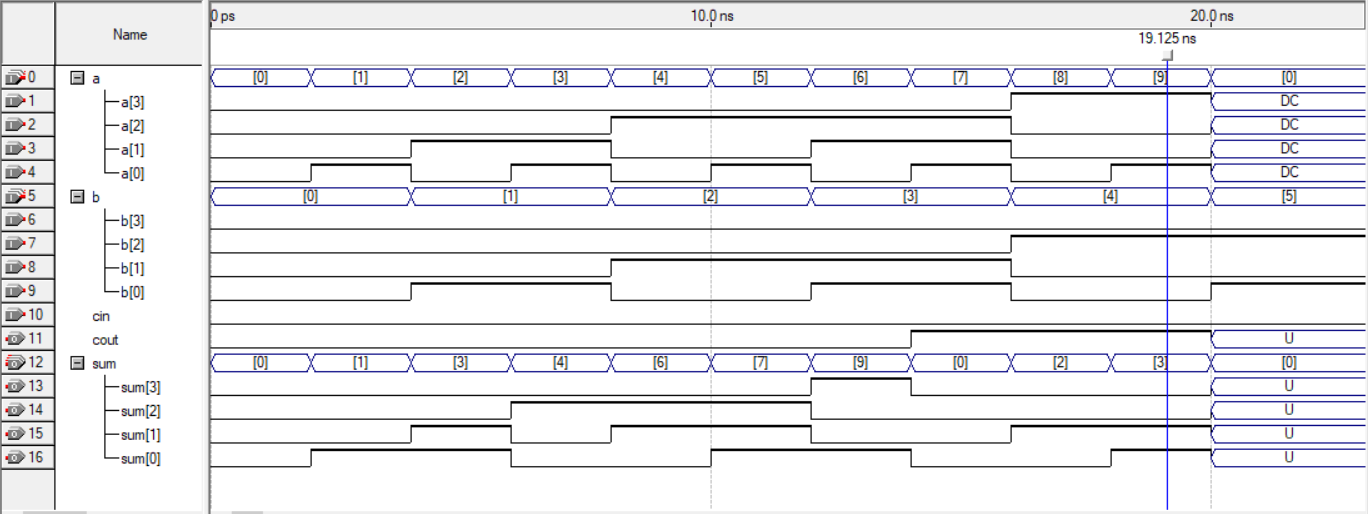


Figure : BCD Adder Waves

When we take a is 0010 (2 in BCD), b is 0001 (1 in BCD), we get -> sum = 0011 and carry(c0) = 0. And that’s true.

When we take a is 1000 (8 in BCD), b is 0100 (4 in BCD), we get -> sum = 0010 and carry(c0) = 1. And that’s true.

### **The Whole System:**

After we connect and integrate the whole system components using structural model, we got the BCD adder-subtractor.

The circuit works as follows: Assume we have two BCD numbers of 4bits A and B, the circuit take the 9’s comp of B using 9’s Complementer, then it choose between B and 9’s Comp B using quadruple 2X1 multiplexer. Then, it calculate the sum of A and the chosen number from the mux using BCD adder which it take two BCD numbers and cin, and it outputs sum and carry.

If the Mode (M) is 0, the quadruple 2X1 multiplexer will choose the number B and cin will be 0, so it finds A+B (When M is 0 it works as an adder).

If the Mode (M) is 1, the quadruple 2X1 multiplexer will choose the 9’s comp B and cin will be 1, so it finds (A + 9’s comp B + 1), which is equals to the subtraction of A and B (A-B).

##### **Block Diagram:**

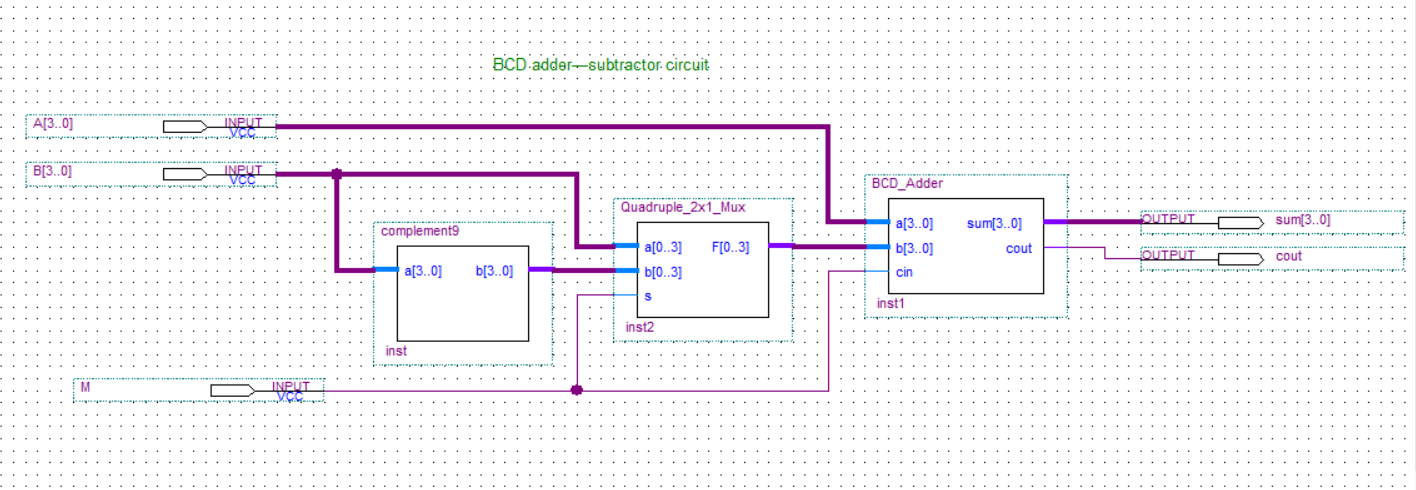
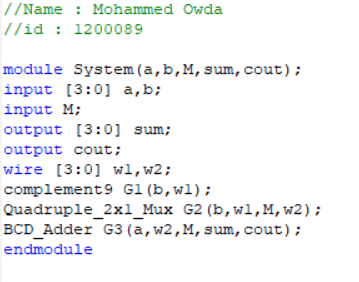
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Figure : BCD Adder-subtractor Block Diagram

##### **Code:**



##### **Simulation:**

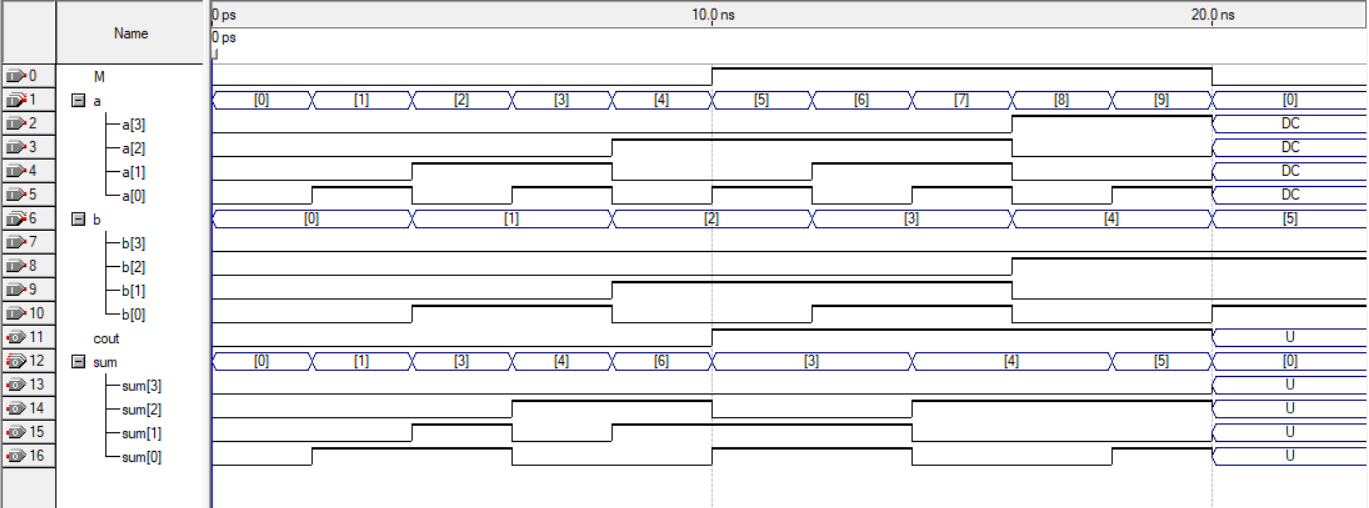
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Figure : BCD adder-subtractor Waves ( The Whole system waves)

When we take the mode (M) = 0, a=0100 and b=0010, we get sum= 0110 and carry=0, which is equals to a + b. And that’s true.

When we take the mode (M) = 1, a=0111 and b=0011, we get sum= 0100 and carry=1, the carry discarded, then the outputs equals to a - b. And that’s true.